

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,743,223 B2  
APPLICATION NO. : 10/643742  
DATED : June 22, 2010  
INVENTOR(S) : Steven L. Scott et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item (56), under "Other Publications", in column 2, line 1, delete "Tthe" and insert -- The --, therefor.

In column 2, line 52, delete "10/643,585" and insert -- 10/643,586 --, therefor.

In column 2, line 52, delete ""Decoupled Vector Architecture"," and insert -- "Decoupled Scalar/Vector Computer Architecture System and Method", --, therefor.

In column 2, line 64, delete "10/643,585," and insert -- 10/643,586, --, therefor.

In column 2, line 65, delete ""Decoupled Vector Architecture"," and insert -- "Decoupled Scalar/Vector Computer Architecture System and Method", --, therefor.

In column 5, line 20, delete "in" and insert -- is --, therefor.

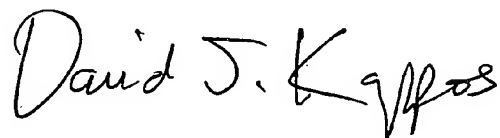
In column 6, lines 29-38, delete "In one embodiment, global memory 26 as shown in FIG. 3 is distributed to each MSP 30 as local memory (not shown in FIGS.). In one embodiment, local memory is packaged as a separate chip (termed the "M" chip as shown in FIG. 4. block 26). Each Ecache 24 has four ports 34 to M chip 26 and connected through M chip 26 to local memory. In one embodiment, ports 34 are 16 data bits in each direction. MSP 30 has a total of 25.6 GB/s load bandwidth and 12.8-20.5 GB/s store bandwidth (depending upon stride) to local memory." and insert -- In one embodiment, global memory 26 as shown in FIG. 3 is distributed to each MSP 30 as local memory (not shown in FIGS.). In one embodiment, local memory is packaged as a separate chip (termed the "M" chip as shown in FIG. 4. block 26). Each Ecache 24 has four ports 34 to M chip 26 and connected through M chip 26 to local memory. In one embodiment, ports 34 are 16 data bits in each direction. MSP 30 has a total of 25.6 GB/s load bandwidth and 12.8-20.5 GB/s store bandwidth (depending upon stride) to local memory. --, below "stores." as a new paragraph.

In column 8, line 29, in Claim 1, delete "connected to" and insert -- connected --, therefor.

In column 8, line 29, in Claim 1, after "network" insert -- to --.

Signed and Sealed this

Seventh Day of September, 2010



David J. Kappos  
*Director of the United States Patent and Trademark Office*

In column 8, line 64, in Claim 4, delete “request” and insert -- requests --, therefor.

In column 9, line 1, in Claim 4, delete “in” and insert -- in the --, therefor.

In column 9, line 7, in Claim 5, delete “request” and insert -- requests --, therefor.

In column 9, line 12, in Claim 5, delete “in” and insert -- in the --, therefor.

In column 9, line 19, in Claim 6, delete “request” and insert -- requests --, therefor.

In column 9, line 31, in Claim 8, delete “request” and insert -- requests --, therefor.

In column 9, line 49, in Claim 10, after “the” insert -- first --.

In column 11, line 37, in Claim 24, delete “subsequent” and insert -- subsequent --, therefor.

In column 12, lines 45-46, in Claim 31, after “memory.” delete “request is received and written by the shared memory.”

In column 12, line 59, in Claim 32, after “the” insert -- write --.

In column 14, line 8, in Claim 35, after “the” insert -- write --.